# Delay Optimization Of Anterior Encryption Radix 8 Multiplier Gimbaled Of Non Redundant Architecture

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## Abstract

In this paper ,introduced a multiplier of anterior encryption radix-8 multiplier gimbaled of non redundant architecture, multipliers are very useful for digital signal processing and audio and video coding and decoding applications, so it may function based on signed as well as unsigned digits. the new followed designed architecture is non redundant radix 4 here the total power and area both are high so in order to decrease the values of existing method here in proposed system of anterior encryption radix-8 multiplier gimbaled of non redundant architecture, encryption method is changed, and number of partial products are decreased and uses the co efficient of +4 to -4 so due to this the , area, delay and power are decreases.

**Keywords: RADIX 8 encoder, partial products generation, CSA Adder ,CLA Adder.**

## Introduction

Following accepted customs and proprieties digital signal applications are improved day by day for example in digital signal processing applications multipliers are mostly used due to this the over all area and processing time is decreased drastically[2] .basically this approach can be approach in all high performance and low power designs. the multiplier is a basic component in DSP applications and those coefficients are not changed even during the execution of application its all is depends on effective architecture.

At firstly the inputs data is encoded by decreasing the non zero digits using canonical signed digit representation (CSD) due this the switching action is decreased but it is hard wired to the specific coefficients and also have some drawbacks so ROM is used to store the outputs for all possible inputs so the computational circuits area and power both are reduced [1] and the partial products are very important for multiplier implementation in booth multiplier the partial products can be reduced to half but these generation is very complex so in order to reduce the partial products complexity used butterfly implementation units of FFT processors by using standard coefficients those stored in ROM [ .For this a newly present system non redundant radix -4 is used with fixed coefficients {-1,0,+1,+2} or {-2,-1,0,+1}[1].in this maximum amount of ROM area is decreased up to each digit request 3 encoding bits per to be stored in ROM. But its required power ,area and delay are high so in order to decrease area ,delay and power the grouping of bits are increased so these 3 parameters are decreased by changing the encoding scheme in non redundant architecture .

# I. Design Multiplier architecture

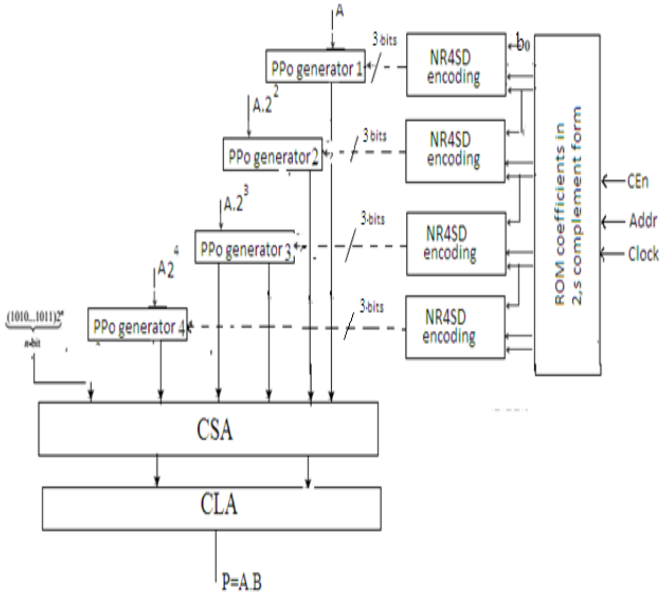


Fig1: block diagram of RADIX-4 multiplier

### *ARCHITECTURE:*

First the chip enable ,address and clock those are used to provide the coefficients which in 2's complement form to multiply two inputs A.B here B is applied to the encoder from the ROM b is nothing but (b0,b1,b2…..bn,bn-1) this the input is encoded and then multiplied by (A0,A1,A2,A3……An) the k partial products those outputs are summed by using CSA adder (carry select adder) its adds the all partial products here the extra bits are added to this CSA adder to shaping the multiplication .here the MSB bit of first partial product is 1 reaming bits also 1 for shaping CSA adder adds partial products and separate the carry and sum and then these outputs gives to the CLA adder (carry look ahead adder )this produces the final addition of carry and sum if the MSB bit is 1 then the product is sign product or its MSB bit is 0 the product is unsigned product .

For encoding grouping is essential here RADIX-4 grouping is presented for entire 10 bits can be get 5 partial products for non redundant RADIX -4 there is 5 partial products and their co efficient are (-1,0,+1,+2), or (-2,-1,0,+1). The coefficient are can be calculated depends on 1 previous bit here non redundant coefficient are used depends on the formulas as show in below . Here $n^+_{2j+1}$ represents one of the input bit like b1 and $n^-_{2j}$ it means b2 the extra bit is taken like previous bit that is acts as bo bit

$$one^+_j = n^+_{2j+1} \wedge n^-_{2j},$$
$$one^-_j = \overline{n^+_{2j+1}} \wedge n^-_{2j},$$
$$two^+_j = n^+_{2j+1} \wedge \overline{n^-_{2j}}.$$

### *PROPOSED SYSTEM:*

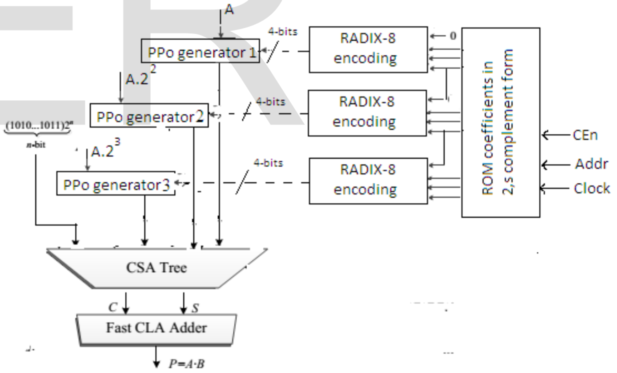


Fig2: architecture of proposed system of RADIX-8

The above proposed system the grouping is changed due to this the power, area and delay will reduced calculation process is also simply the encoding technique used here is RADIX-8.same algorithm is applied the number of partial products are reduced up to n/3 here n represents number of multiplier bits applied at encoder input .depends on final output the signed and unsigned both can be recognized by their MSB bits like existing system

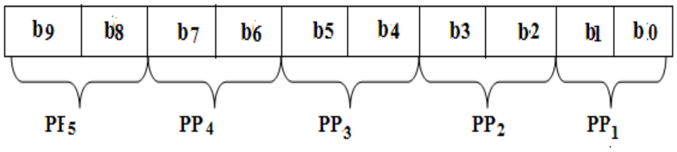


Fig3: grouping of bits in RADIX-4

The entire bits is grouped in to 3 bits one bit is overlapped with another group so for existing system the input bits are 10 bits are considered 8 are input bits reaming are previous bits consider as MSB bits for completion of grouping .

Table 1

RADIX-4 recodings

| Multiplier bits | | | Coeffients in encoding |
|---|---|---|---|
| y2 | y1 | y0 | |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | +1 |
| 0 | 1 | 0 | +1 |
| 0 | 1 | 1 | - 2 |
| 1 | 0 | 0 | -2 |
| 1 | 0 | 1 | -1 |
| 1 | 1 | 0 | -1 |
| 1 | 1 | 1 | 0 |

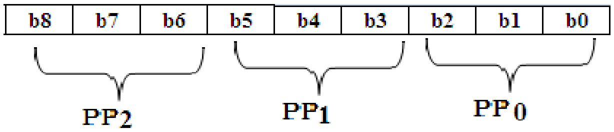


Fig 4: grouping of RADIX -8

The input multiplier bits are 8 those are 4 bits are grouped together the one bit is overlapped with another group so the required partial products are 3 the grouping of bits are show in above here the one extra previous bit is consider as a MSB bit for completion of grouping.

Table -2

RADIX-8 recoding

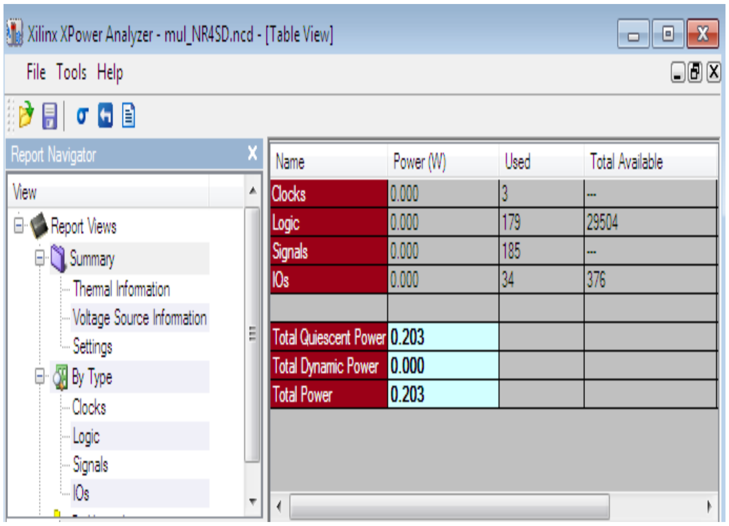
| Multiplier values | | | | encoded Coeffients |
|---|---|---|---|---|
| b0 | b1 | b2 | b3 | |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | +1 |
| 0 | 0 | 1 | 0 | +1 |
| 0 | 0 | 1 | 1 | +2 |
| 0 | 1 | 0 | 0 | +2 |
| 0 | 1 | 0 | 1 | +3 |
| 0 | 1 | 1 | 0 | +3 |
| 0 | 1 | 1 | 1 | +4 |
| 1 | 0 | 0 | 0 | -4 |
| 1 | 0 | 0 | 1 | -3 |
| 1 | 0 | 1 | 0 | -3 |
| 1 | 0 | 1 | 1 | -2 |
| 1 | 1 | 0 | 0 | -2 |
| 1 | 1 | 0 | 1 | -1 |
| 1 | 1 | 1 | 0 | -1 |
| 1 | 1 | 1 | 1 | 0 |

## *PARTIAL PRODUCT GENERATION:*

The partial products are generated like here the multiplicand is multiplied by the coefficients of 0,+1,+2,+3,+4,-1,-2,-3,-4.if the coefficient is 0 the multiplicand is multiplied by 0.if it is 1 the product is same as like multiplicand value .if the coefficients is -1 the product value is 2's complement form of the value. For -2 its shifts left by 1 bit and 2'complement form of the multiplicand value if it is 2 simply shift left by one bit .for -4 the multiplicand is shift left by 2 bits and perform 2's complement and multiply by 2 that is shift left to 2 bits .for 3 we can just add 2Y and 1Y .due to this the transition time will decrease and the manufacturing transistors are also decreased.

The overall there 3 partial products are given to the CSA adder it produce the sum and carry separately for perfect shaping of multiplication the extra added bits are added to this adding process both outputs are given to CLA adder here the output is final product .

## II. SIMULATION RESULTS OF RADIX-4



| Name | Power (W) | Used | Total Available |
|---|---|---|---|
| Clocks | 0.000 | 3 | -- |
| Logic | 0.000 | 179 | 29504 |
| Signals | 0.000 | 185 | -- |
| IOs | 0.000 | 34 | 376 |
| | | | |
| Total Quiescent Power | 0.203 | | |
| Total Dynamic Power | 0.000 | | |
| Total Power | 0.203 | | |

Fig5: The XPower analyzer report for existing method having the power of 0.2 watts

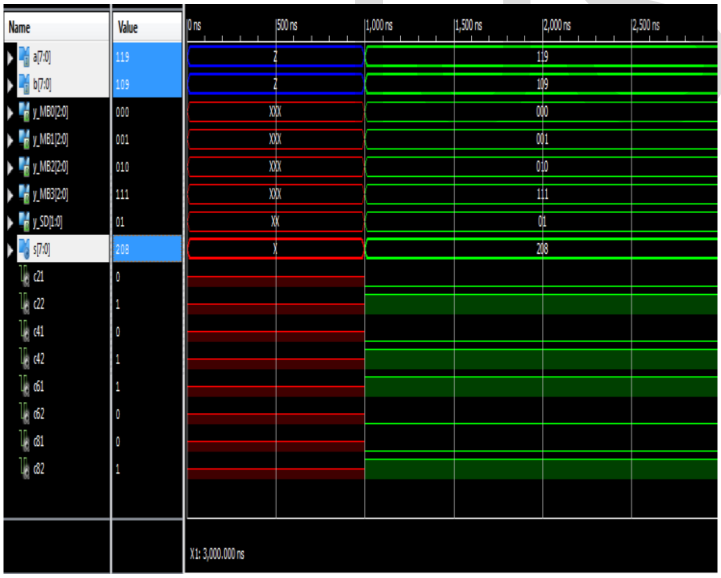


Fig6: Simulation results for X=119, and Y =109 those in decimal form and their related partial products

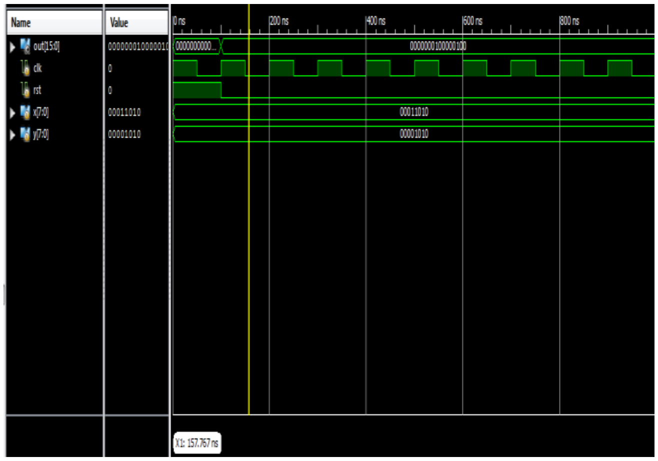
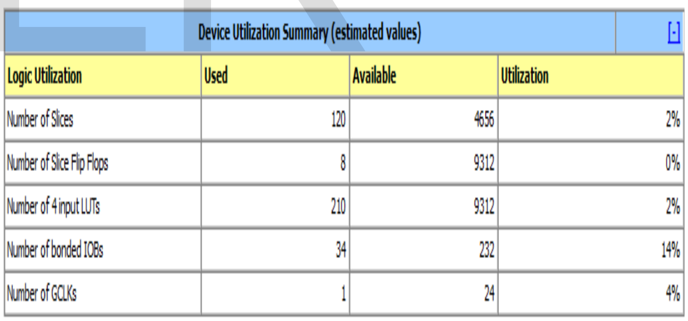


Fig7: simulation results for X=00011010,y=00001010 for this the resultant output value is out(15):0000000100000100 for clock 0,reset 0

In above grouping the 4 partial products are required and the total power required for the device is 0.203 watts and area is show in table

Table-3

Device utilization for RADIX-4



Device Utilization Summary (estimated values)

| Logic Utilization | Used | Available | Utilization |
|---|---|---|---|
| Number of Slices | 120 | 4656 | 2% |
| Number of Slice Flip Flops | 8 | 9312 | 0% |
| Number of 4 input LUTs | 210 | 9312 | 2% |
| Number of bonded IOBs | 34 | 232 | 14% |
| Number of GCLKs | 1 | 24 | 4% |

***Timing Summary for RADIX-4:***

Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: 19.864ns
Maximum output required time after clock: 4.040ns
Maximum combinational path delay: No path found

***Timing Detail:***

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```
All values displayed in nanoseconds (ns)
=========================================
==================================
Timing constraint: Default OFFSET IN BEFORE for
Clock 'clk'
  Total number of paths / destination ports: 156353 / 30
-------------------------------------------------------------------
-----
Offset:              19.864ns (Levels of Logic = 17)
  Source:            y<2> (PAD)
  Destination:       out_14 (FF)
  Destination Clock: clk rising
  Data Path: y<2> to out_14
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name
(Net Name)
    ----------------------------------------  ------------
     IBUF:I->O           27   1.106   1.141  y_2_IBUF
(y_2_IBUF)
     LUT3:I1->O          12   0.612   0.886
m1/m3/Madd_digit_Madd_xor<1>111 (N2)
     LUT3:I1->O           1   0.612   0.000
m1/m4/Madd_digit_Madd_xor<0>1111
(m1/m4/Madd_digit_Madd_xor<0>111)
     MUXF5:I1->O         10   0.278   0.902
m1/m4/Madd_digit_Madd_xor<0>111_f5 (N11)
     LUT3:I0->O          12   0.612   0.847
m1/m4/Madd_digit_Madd_xor<1>11 (y4<1>)
     LUT4:I2->O           1   0.612   0.387
m2/pp4<8>_SW2 (N78)
     LUT4:I2->O           3   0.612   0.520  m2/pp4<8>
(pp4<8>)
     LUT4:I1->O           1   0.612   0.000
m3/Madd_p2_lut<8> (m3/Madd_p2_lut<8>)
     XORCY:LI->O          4   0.458   0.651
m3/Madd_p2_xor<8> (m3/p2<8>)
     LUT2:I0->O           2   0.612   0.449
m3/m3/Mxor_s_Result<8>1 (s<8>)
     LUT4:I1->O           3   0.612   0.603  m4/c91 (m4/c9)
     LUT4:I0->O           3   0.612   0.603  m4/c101
(m4/c10)
     LUT4:I0->O           3   0.612   0.603  m4/c111
(m4/c11)
     LUT4:I0->O           3   0.612   0.603  m4/c121
(m4/c12)
     LUT4:I0->O           3   0.612   0.603  m4/c131
(m4/c13)
     LUT4:I0->O           1   0.612   0.387  m4/c141
(m4/c14)
     LUT4:I2->O           1   0.612   0.000  z<14>1
(z<14>)
     FDR:D                    0.268          out_14
    ----------------------------------------
    Total                19.864ns (10.678ns logic, 9.186ns
route)
                               (53.8% logic, 46.2% route)
```

And the Total delay is 19.864ns (10.678ns logic, 9.186ns route) (53.8% logic, 46.2% route)

## III. SIMULATION RESULTS OF RADIX-8

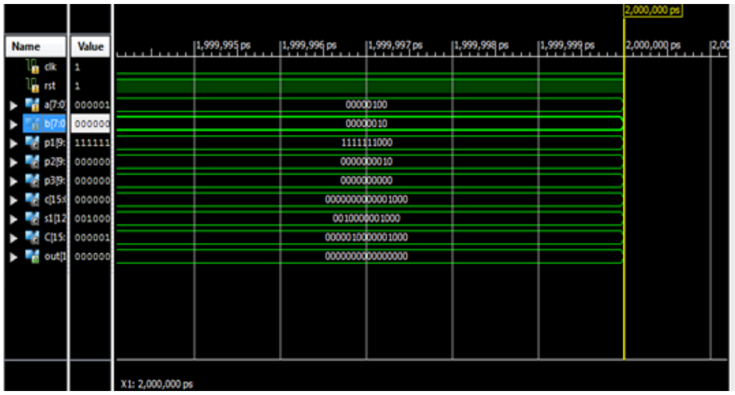
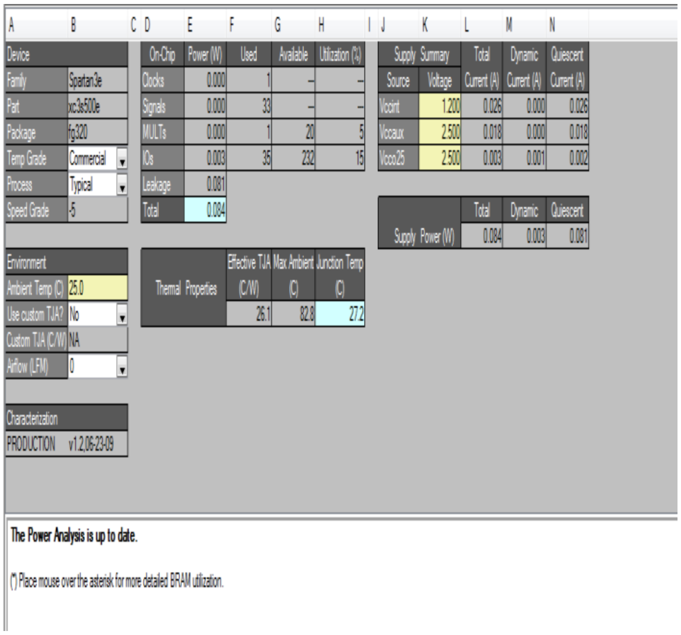


Fig8: Simulation results a=00000100,y=00000010 and out(15):0000000000001000 for clock 0 and reset 0



| A | B | C | D | E | F | G | H |
|---|---|---|---|---|---|---|---|
| Device | | | On-Chip | Power (W) | Used | Available | Utilization (%) |
| Family | Spartan3e | | Clocks | 0.000 | 1 | --- | --- |
| Part | xc3s500e | | Signals | 0.000 | 33 | --- | --- |
| Package | fg320 | | MULTs | 0.000 | 1 | 20 | 5 |
| Temp Grade | Commercial | | IOs | 0.003 | 35 | 232 | 15 |
| Process | Typical | | Leakage | 0.081 | | | |
| Speed Grade | -5 | | Total | 0.084 | | | |

| J | K | L | M | N |
|---|---|---|---|---|
| Supply Summary | | Total | Dynamic | Quiescent |
| Source | Voltage | Current (A) | Current (A) | Current (A) |
| Vccint | 1.200 | 0.026 | 0.000 | 0.026 |
| Vccaux | 2.500 | 0.018 | 0.000 | 0.018 |
| Vcco25 | 2.500 | 0.003 | 0.001 | 0.002 |

| | Total | Dynamic | Quiescent |
|---|---|---|---|
| Supply Power (W) | 0.084 | 0.003 | 0.081 |

| Environment | |
|---|---|
| Ambient Temp (C) | 25.0 |
| Use custom TJA? | No |
| Custom TJA (C/W) | NA |
| Airflow (LFM) | 0 |

| Thermal Properties | Effective TJA (C/W) | Max Ambient (C) | Junction Temp (C) |
|---|---|---|---|
| | 26.1 | 82.8 | 27.2 |

| Characterization | |
|---|---|
| PRODUCTION | v1.2,06-23-09 |

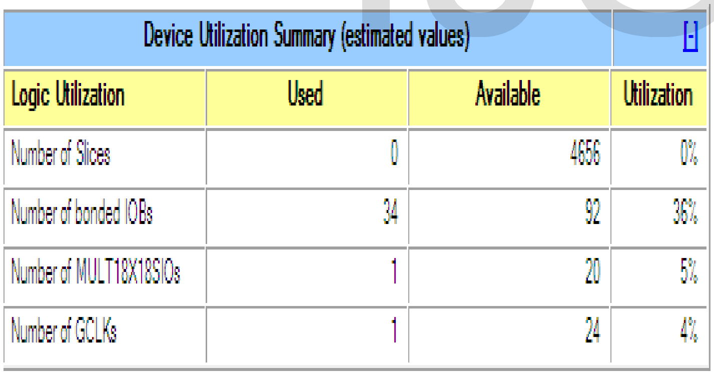
The Power Analysis is up to date.

(*) Place mouse over the asterisk for more detailed BRAM utilization.

Fig:9 Power report of RADIX-8

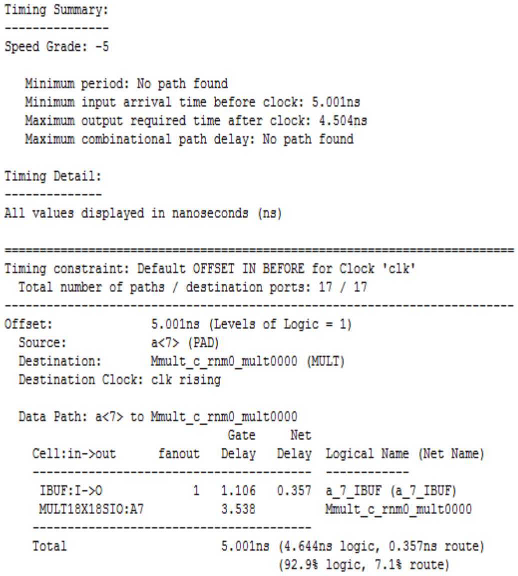
Table 4

Device utilization for RADIX-8



| Device Utilization Summary (estimated values) | | | [-] |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 0 | 4656 | 0% |
| Number of bonded IOBs | 34 | 92 | 36% |
| Number of MULT18X18SIOs | 1 | 20 | 5% |
| Number of GCLKs | 1 | 24 | 4% |

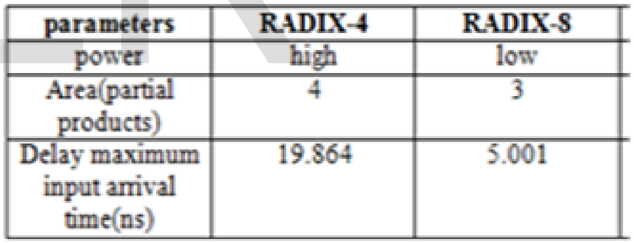
***Timing reports for RADIX-8:***



```
Timing Summary:
---------------
Speed Grade: -5

   Minimum period: No path found
   Minimum input arrival time before clock: 5.001ns
   Maximum output required time after clock: 4.504ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 17 / 17
-------------------------------------------------------------------------
Offset:              5.001ns (Levels of Logic = 1)
  Source:            a<7> (PAD)
  Destination:       Mmult_c_rnm0_mult0000 (MULT)
  Destination Clock: clk rising

  Data Path: a<7> to Mmult_c_rnm0_mult0000
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.106   0.357  a_7_IBUF (a_7_IBUF)
     MULT18X18SIO:A7           3.538          Mmult_c_rnm0_mult0000
    ----------------------------------------
    Total                      5.001ns (4.644ns logic, 0.357ns route)
                                       (92.9% logic, 7.1% route)
```

## V.COMPARISON OF RADIX-4 AND RADIX-8

Table-5



| parameters | RADIX-4 | RADIX-8 |
|---|---|---|
| power | high | low |
| Area(partial products) | 4 | 3 |
| Delay maximum input arrival time(ns) | 19.864 | 5.001 |

## V.CONCLUSION:

The Anterior encryption radix 8 multiplier Gimbaled of Non redundant Architecture has simulated by using Xilinx 13.1 simulators using the device of xc3s500e –fg320 package .the RADIX-8 generates 3 partial products and total cycling time and power are reduces highly the main components are carry save adder and carry lock ahead adder(CLA) those are used to increase the speed of operation the final product is come from the CLA adder hardware implementation is decreased highly as comparative RADIX-4.

### *REFFERENCE:*

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